* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the bit synchronization equipment which extracts synchronous timing from a bit synchronization signal, and establishes a bit synchronization.
[0002]
[Description of the Prior Art] Conventionally, the synchronous timing of an NRZ (Non Return to Zero) signal is extracted by the circuit as shown in drawing 7 . In this drawing, the edge detector 6 detects the variation-of-sign point of the NRZ signal S1 shown in drawing 8 , and outputs the edge detecting signal S5 which consists of a pulse with narrow width of face in the standup and falling of the NRZ signal S1. The timing tank 7 is a resonance circuit which has center frequency equal to the bit rate of the NRZ signal S1, and since it answers a signal S5 from the edge detector 6 and carries out damping oscillation, it can compensate the clock of a part without the variation-of-sign point in the NRZ signal S1. Corrugating of the output signal S6 of the timing tank 7 is carried out by the limiter 8, jitter oppression is carried out by the phase locked loop (PLL) 9, and the output signal S7 is supplied to CPU10 as a timing clock signal S8. Based on this clock signal S8, CPU10 samples the NRZ signal S1, and accumulates a result in the data storage section.
[0003] In addition, when the Q value of the timing tank 7 can take highly, in order for timing tank 7 self to have the oppression effectiveness of a jitter, PLL9 may be omitted and the output signal S7 of a limiter 8 may be used as a timing clock as it is.
[0004]
[Problem(s) to be Solved by the Invention] However, in performing a digital data communication link at the low speed of dozens of kilobits from hundreds of bits in 1 second, the center frequency of the timing tank 7 is low, and it becomes difficult to obtain Q value high enough. That is, if (1) timing tank is constituted from a passive element, both an inductance and capacitance serve as a big value, and the configuration of a component will become large and will become expensive. Moreover, high Q value of the component itself cannot be taken.
(2) if the timing tank is equivalent to a band pass filter (BPF) if a timing tank is constituted from an active element, and it is going to obtain high Q value -- oscillating -- ****** -- **
[0005] Therefore, the conventional bit synchronization equipment using a timing tank is unsuitable for low-speed data transmission. Moreover, it is difficult to generate a timing clock only from a several bits bit synchronization signal on the configuration with conventional bit synchronization equipment.
[0006] The purpose of this invention is to offer the bit synchronization equipment which is an easy configuration, and can extract synchronous timing certainly, and can moreover extract synchronous timing from the bit synchronization signal for several bits, even when such a problem is solved and data are transmitted at a low speed.
[0007]
[Means for Solving the Problem] The purpose of this invention is bit synchronization equipment which extracts synchronous timing from the bit synchronization signal which is added in front of transmit data

and sent serially, and establishes a bit synchronization. An edge detection means to sample said synchronizing signal at a rate quicker than the bit rate of said bit synchronization signal, and to detect the variation-of-sign point of said synchronizing signal, The count of the sampling which makes a reference point one of the detected variation-of-sign points, and is performed between this reference point and each variation-of-sign point, A jitter measurement means to compute the average value of a difference with the count of the sampling performed between said reference point and each variation-of-sign point when there is no jitter in said bit synchronization signal, It is attained by the bit synchronization equipment characterized by having a synchronous set means to set a sampling start point as the bit rate of said transmit data using said computed average that said transmit data should be sampled an equal period substantially at the core of each bit.

[0008]

[Function] It is added in front of transmit data, and the bit synchronization signal sent serially is sampled at the rate several times the rate of a bit synchronization by the edge detection means, and a variation-of-sign point is detected. A jitter measurement means makes an origin/datum one of the variation-of-sign points detected by the edge detection means, and computes the average of the difference of the count of a sampling between this origin/datum and each variation-of-sign point, and the count of a sampling which should be performed between said origin/datum and each variation-of-sign point when a jitter is not contained in a bit synchronization signal. A synchronous set means sets up a sampling start point using the computed average, and sets up the sampling period of a sampling timer almost equally to this equally to the bit rate of transmit data. Thus, it is added in front of transmit data, and the average value of a jitter is detected based on the bit synchronization signal sent serially, and when only this average value shifts a sampling start point, a jitter component is amended, and the data signal sent following a bit synchronization signal is sampled at the core.

[0009]

[Example] Next, the example of this invention is explained to a detail with reference to a drawing. The block diagram of the bit synchronization equipment by this invention is shown in drawing 1 . This bit synchronization equipment is constituted by CPU1. In this drawing, the sampling timer 11 generates and outputs the sampling pulse which has a bit rate 6 times the frequency T1 of the bit synchronization signal inputted into this bit synchronization equipment, and the sampling pulse T2 which has the same or frequency T2 almost equal to this as the bit rate of a bit synchronization signal. The phase of a sampling pulse T2 is set up based on the below-mentioned delay signal S4.

[0010] The edge detection routine 2 samples a bit synchronization signal to the timing of the sampling pulse of a frequency T1, and detects the variation-of-sign point. The jitter measurement routine 3 makes an origin/datum one of the variation-of-sign points which the edge detection routine 2 detected, searches for the number of the sampling pulses contained before each variation-of-sign point which the edge detection routine 2 detected from the origin/datum, and a number of a sampling pulse of differences which are contained from an origin/datum before each variation-of-sign point when there is no jitter in a bit synchronization signal, and computes the average. The synchronous set routine 4 generates delay signal S4 based on the average which the jitter measurement routine 3 computed, supplies this to the sampling timer 11, and sets up the phase of the sampling pulse of a frequency T2. The data storage section 5 carries out a received-data sampling to the timing of the sampling pulse of a frequency T2, and accumulates the sampled received data.

[0011] The gap with each variation-of-sign point of the bit synchronization signal of a sending signal and each variation-of-sign point of the bit synchronization signal of an input signal, i.e., jitter component deltati, is shown by the degree type.

[0012]

[Equation 1]

$$\Delta t i = t i' - (t i + A)$$

[0013] Here, i is the number of a variation-of-sign point, ti expresses the time of day of each variation-of-sign point of the bit synchronization signal of a sending signal, and ti' expresses the time of day of

each variation-of-sign point of the bit synchronization signal of an input signal. Moreover, A expresses the average of a jitter component. The time of day ti of the point changing [these] and the relation of ti' come to be shown in drawing 3 , when a point (ti, ti') is plotted on the graph with which it was shown in drawing 2 , and the axis of abscissa was made to t and they made the axis of ordinate t'. A continuous line is a straight line expressed with t'=t+A among drawing, and the point (ti, ti') varies focusing on this straight line.

[0014]

[Equation 2]

$$\sum_{i=1}^{n} \Delta ti = \frac{1}{n}\sum_{i=1}^{n} (ti' - ti' - A)$$

$$= \frac{1}{n}\left[\sum_{i=1}^{n} (ti' - ti) - \sum_{i=1}^{n} A\right]$$

$$= \frac{1}{n}\sum_{i=1}^{n} (ti' - ti) - A$$

従って

$$A = \frac{1}{n}\sum_{i=1}^{n} (ti' - ti)$$

[0015] By carrying out, it becomes possible to amend a jitter component. The jitter measurement routine 3 computes the average value A of a jitter, and based on that average value A, the synchronous set routine 4 amends the gap accompanying a jitter, and controls the phase of a sampling pulse by this bit synchronization equipment appropriately.

[0016] Next, actuation of the above-mentioned bit synchronization equipment in case the 8-bit bit synchronization signal which consists of bits B1-B8 is added in front of the transmit data is explained with reference to the wave form chart of drawing 4 , and the flow chart of drawing 5 .

[0017] The jitter measurement routine 3 sets the average jitter A, sample number-of-bits B, the sample counter C, and Jitter D as 0 as initial setting of a parameter first, respectively (step S501). Next, the sampling timer 11 sets the frequency of a sampling pulse to a signal 6 times the frequency T1 of a bit synchronization (step S502). If an input signal S1 is inputted in this condition, the edge detection routine 2 samples a signal S1 to the timing of a sampling pulse (step S503), adds 1 to C (step S504), judges whether the sign of a signal S1 changed (step S505), and it will repeat step S503-505 until a sign changes. And change of a sign tells this to the jitter measurement routine 3.

[0018] Thereby, the jitter measurement routine 3 sets B and C as 1 as a setup of a reference point first, respectively (step S506). Then, if the edge detection routine 2 performs the same processing as step S503-505, and performs edge detection of an input signal S1, therefore a bit synchronization signal and an edge is detected, it will be given to the jitter measurement routine 3 by making several C into the signal S2 of the sampling pulse counted by then (step S507). Several C of this sampling pulse is equal to the number of the sampling pulses contained from the origin/datum which is the timing of the standup of the bit B1 of a bit synchronization signal before falling of a bit B1 (refer to drawing 4).

[0019] The jitter measurement routine 3 computes Jitter D by D=C-6xB (step S508). In this formula, 6xB is the number of the sampling pulses originally contained from the standup of a bit B1 before falling (in this case, 6), when there is no jitter in an input signal S1. Therefore, D serves as the number of the sampling pulses contained at the period deltat1 shown in drawing 4 .

6×B=Threshold

[0020] Next, the jitter measurement routine 3 adds 1 to number-of-bits B (step S509), and waits to send a signal S2 from the edge detection routine 2. And the edge detection routine 2 detects the standup of bit B-2, and if several C is outputted as a signal S2 of the sampling pulse which carried out counting by

then (step S510), the jitter measurement routine 3 will compute the number of the sampling pulses contained at the jitter deltat2 corresponding to the standup of bit B-2, i.e., a period, like the case of a bit B1 (step S511).

[0021] Like the following, each bit B3, falling of B4, and the jitter that corresponds for starting are measured, and the jitter corresponding to falling of bit B5 is measured by step S512-514 also to bit B5.

[0022] The average A of a jitter is calculated by the synchronous set routine's 4 making the jitter for every bit which the jitter measurement routine 3 measured a signal S3, adding all of reception and them in the period of a bit B7 from the jitter measurement routine 3, and dividing by 5 (step S515). In addition, it is as follows when this processing is expressed with a formula.

[0023]

[Equation 3]

ジッタの平均値 $A = 1/5 \cdot \sum_{i=1}^{5} (\Delta t_i$ 中のサンプリングパルスの数$)$ → averaging

[0024] And the number of the sampling pulses contained at the average value A of a jitter and the period of a 1-bit half period, 3 [i.e.,], is added at the time of falling of a bit B8, and signal S4 only for the time amount equivalent to the sampling pulse of the number of the addition results to shift a phase is given to the sampling timer 11 (step S516), and the phase of the sampling pulse of the frequency T2 which the sampling timer 11 outputs is set up (step S517). Consequently, the timing of the sampling pulse of a frequency T2 will be set up in the center of each bit of received data.

[0025] The data storage section 5 receives the received data which follow a bit synchronization signal synchronizing with the sampling pulse to which it carried out in this way, and the phase was set (step S518), and repeats the several bits actuation which checks whether the bit synchronization can be taken (step S519).

[0026] Thus, since a timing tank is not used for the bit synchronization equipment of this example, even when performing data transmission at a low speed, a bit synchronization is established certainly and, moreover, it can establish a synchronization with the bit synchronization signal for several bits.

[0027] In addition, if it is not necessary to not necessarily make the frequency of the sampling pulse which the sampling timer 11 outputs to the data storage section 5 in agreement with the frequency of a bit synchronization signal and it is mostly in agreement, the sampling of received data is possible for it. When received data are short, or when a gap of the system clock of CPU can be disregarded That what is necessary is just to input into equipment in the form where received data only follow a bit synchronization signal as an input signal S1 as shown in drawing 6 (a) What is necessary is on the other hand, to divide received data, to add a bit synchronization signal for each [which was divided] received data of every, and just to restart synchronous timing, as shown in drawing 6 (b) when received data are long, or when a gap of the system clock of CPU cannot be disregarded.

[0028]

[Effect of the Invention] The bit synchronization equipment of this invention is comparatively easy to constitute, as explained above, since a timing tank is not used, even when performing data transmission at a low speed, equipment can be constituted cheaply, and a bit synchronization can be established certainly, and moreover, a synchronization can be established with the bit synchronization signal for several bits. Especially the bit synchronization equipment of this invention is the the best for reception of short data, such as a yard paging system.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the bit synchronization equipment by this invention.
[Drawing 2] It is the explanatory view of the relation between the variation-of-sign point of a sending signal, and the variation-of-sign point of an input signal.
[Drawing 3] It is the graph which shows the relation between the variation-of-sign point of a sending signal, and the variation-of-sign point of an input signal.
[Drawing 4] It is a timing chart for explaining actuation of the bit synchronization equipment of drawing 1 .
[Drawing 5] It is a flow chart for explaining actuation of the bit synchronization equipment of drawing 1 .
[Drawing 6] It is drawing showing a format of transmit data.
[Drawing 7] It is the block diagram of conventional bit synchronization equipment.
[Drawing 8] It is the wave form chart showing the signal of each part of the bit synchronization equipment of drawing 7 .
[Description of Notations]
1 CPU
2 Edge Detection Routine
3 Jitter Measurement Routine
4 Synchronous Set Routine
5 Data Storage Section
11 Sampling Timer

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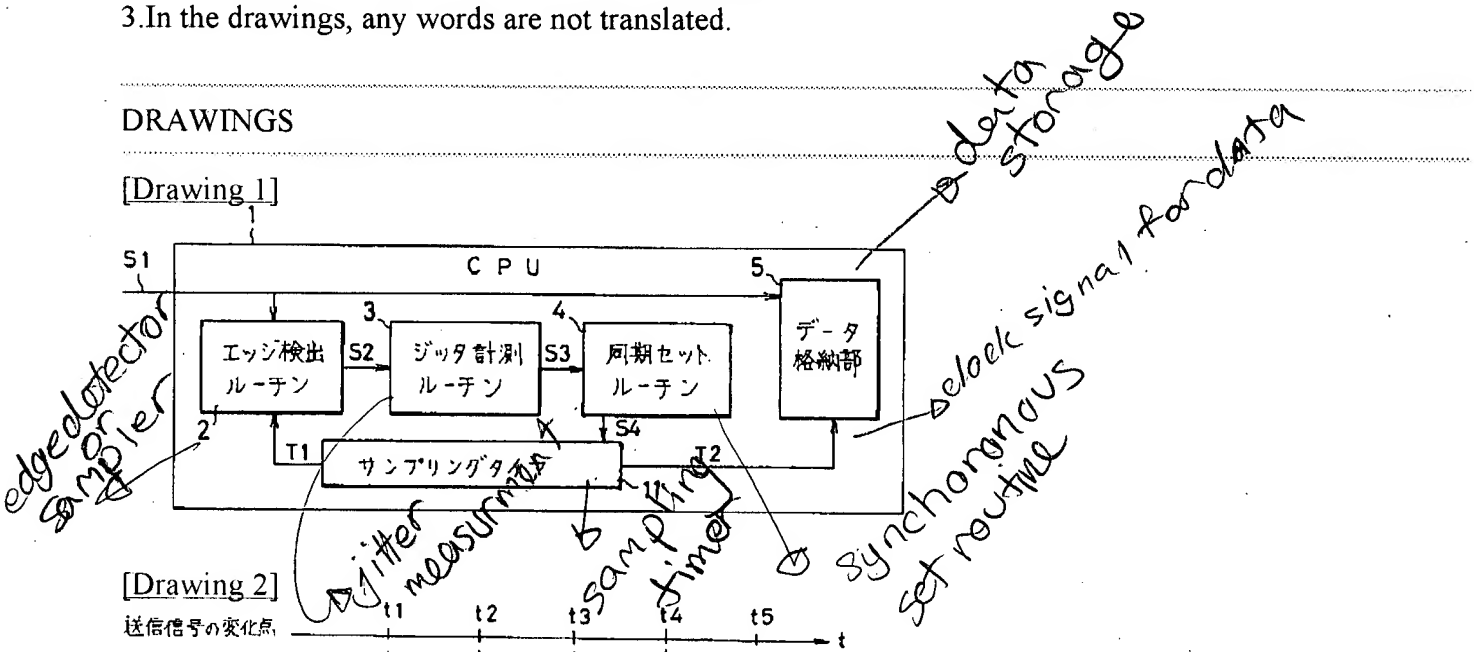
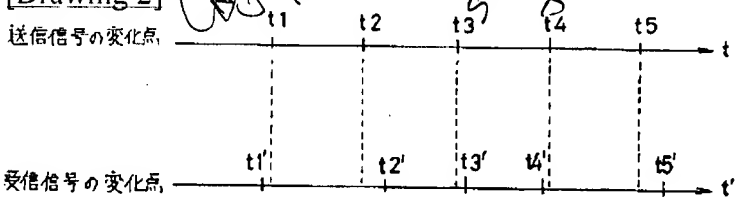
DRAWINGS

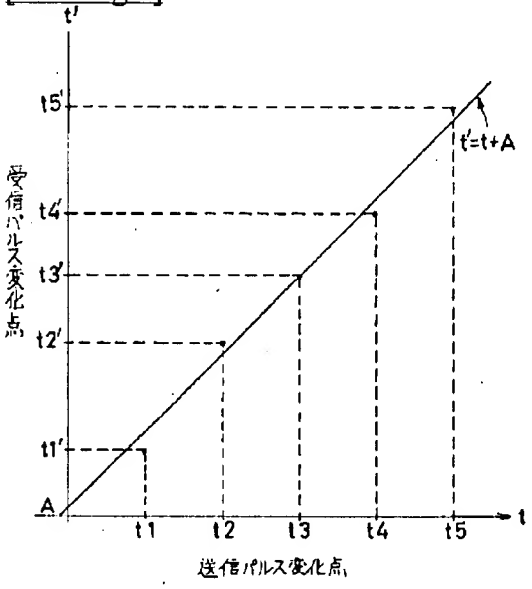
[Drawing 1]



[Drawing 2]

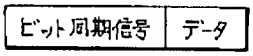


[Drawing 3]

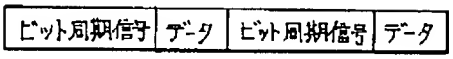


[Drawing 6]

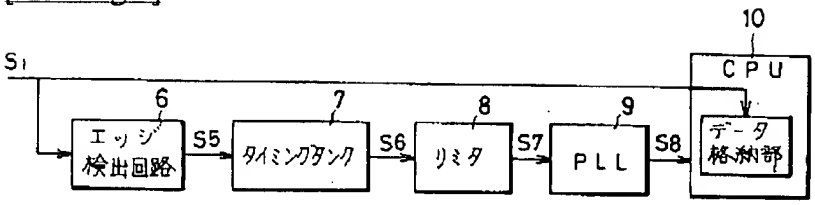
(a)



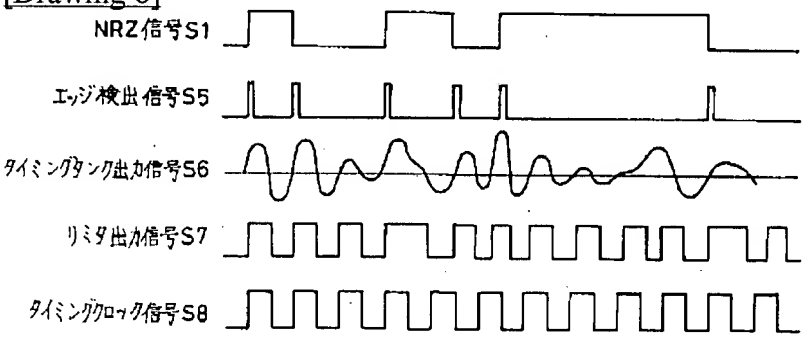
(b)



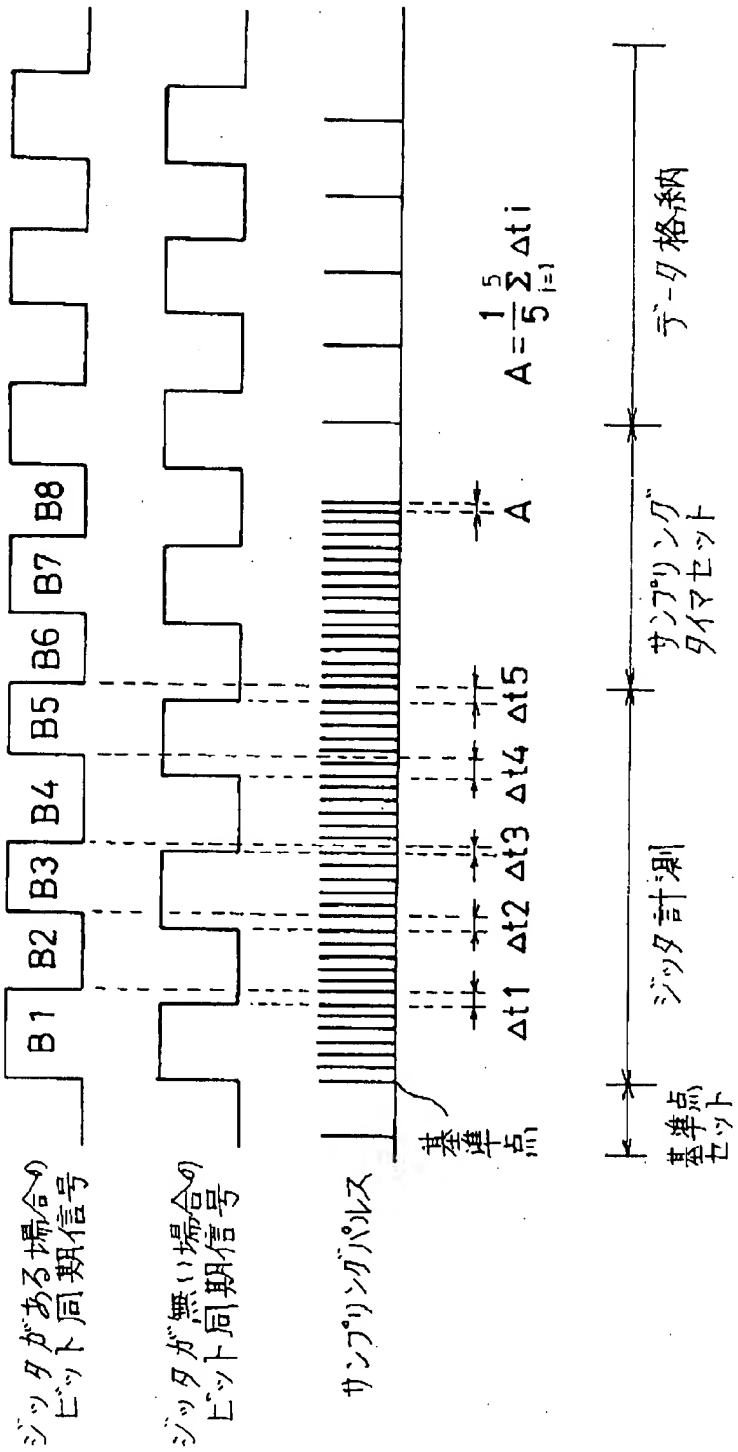
[Drawing 7]



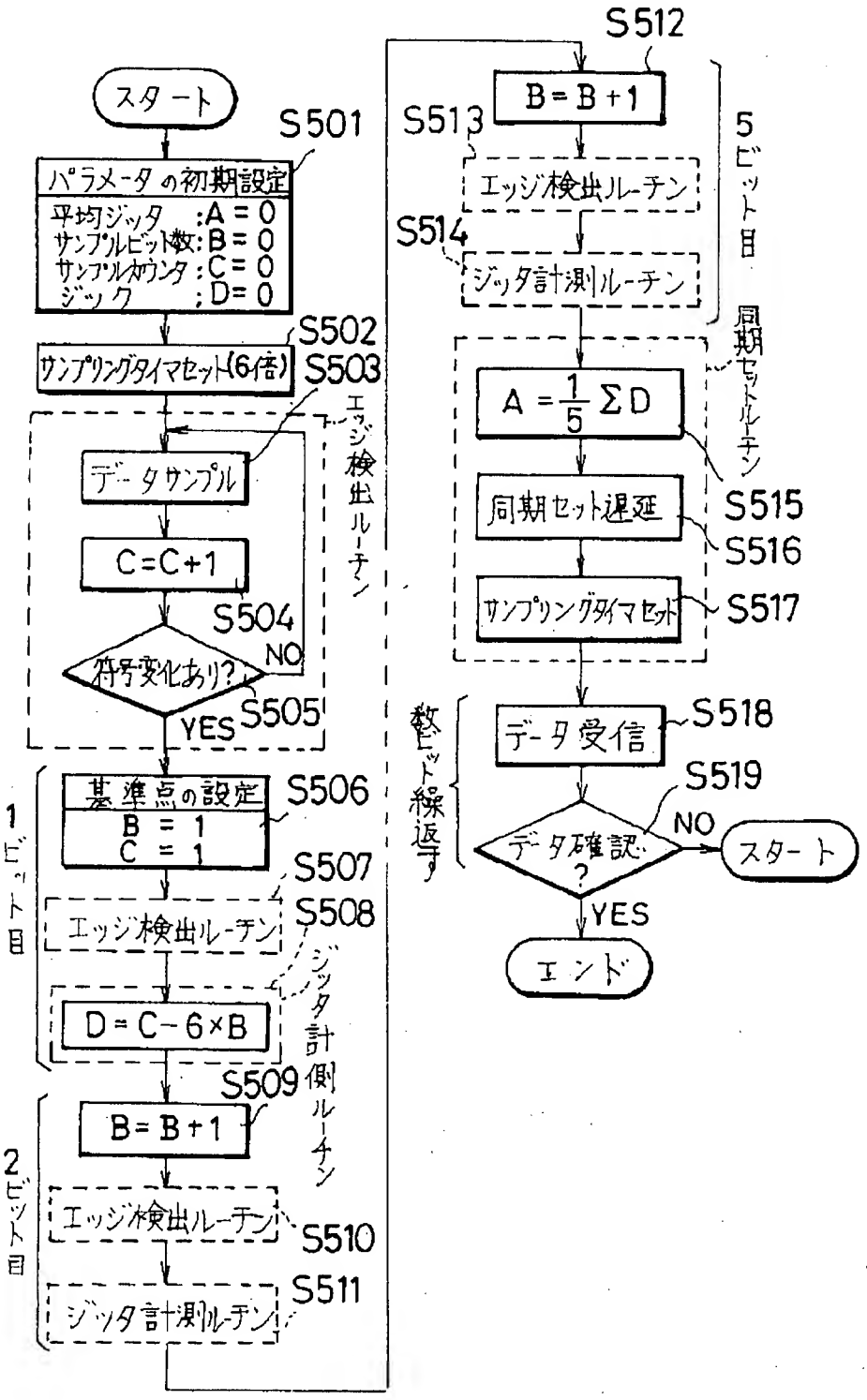
[Drawing 8]



[Drawing 4]


ジッタがある場合のビット同期信号
ジッタが無い場合のビット同期信号
サンプリングパルス
基準点
B1
B2
B3
B4
B5
B6
B7
B8
Δt1
Δt2
Δt3
Δt4
Δt5
A
$A=\frac{1}{5}\sum_{i=1}^{5}\Delta t_i$
基準点セット
ジッタ計測
サンプリング"タイマセット
データ格納

[Drawing 5]



[Translation done.]